(nonzero sampling aperture) make the sampling timing inaccurate. In fact, the bandwidth of a voltage sampling circuit must be much larger than the signal bandwidth. This makes direct sampling of high frequency radio signal extremely difficult. Sub-sampling can reduce the sampling rate but not the bandwidth of the sampling circuit and not the demands on small clock jitter and small sampling aperture.--

line 28, please replace the section heading with --Summary--.

Page 2, line 22, please replace the paragraph beginning at line 22 with the following:

--Another more specific object of the invention is to provide a two-step BPCS circuit. This is achieved by a two-step BPCS circuit according to the invention, which comprises a first BPCS circuit according to the invention for producing signal samples with a first sample rate; a chopping circuit for chopping the signal from the first BPCS circuit symmetrically in time at its signal output or output pair with the frequency of a clock signal equal to the first sample rate; a differential-out amplifier for amplifying the signal from the chopping circuit differentially; wherein the first signal input and the second signal input of said second BPCS are connected to the signal output pair of said amplifier for producing signal samples at the signal output or output pair with a second sample rate.--

Page 3, line 26, please replace the paragraph beginning at line 26 with the following:

--An advantage of the charge sampling circuit according to the invention is that the bandwidth of the charge sampling circuit does not have to be much larger than the signal bandwidth. It is also important that for a radio signal, no matter how high the carrier frequency is, the signal bandwidth (the base band) remains a small fraction of the full bandwidth between DC carrier frequency. It is therefore unnecessary to convert the full bandwidth. Instead, it is only necessary to convert the bandwidth comprising the signal.--

Page 4, line 15, please replace the paragraph beginning at line 15 with the following:

--Both the center frequency and the bandwidth of a BPCS circuit can be easily programmed. The bandwidth can be as narrow as required; equivalent to having an unlimited Q-value.--

C4

Page 6, line 24, please replace with section heading with --Detailed Description--.

Pages 6-7, please replace the paragraph beginning at line 30 with the following:

--With reference to FIG 1A, a first embodiment of a charge sampling (CS) circuit 1 according to the invention is shown. It comprises sampling switch 2, an integrator 3 and a control signal generator 4. The switch 2 has a signal input, a signal output and a control input. An analog signal is applied to the signal input of the switch, which is the signal input of the charge sampling circuit 1, and a sampling signal is applied to the control input from the control signal generator 4. The switch is on, i.e the signal input is connected to the signal output of the switch, only when the sampling signal is in the sampling phase. The integrator 3 has a signal input, a signal output, and a control input. The signal output of the switch 2 is applied to the signal input of the integrator 3, and a resetting signal from the control signal generator 4 is applied to the control input of the integrator 3. The current of the analog input signal to the CS circuit 1 is integrated during the sampling phase, and the integrated charge produces a proportional voltage or current sample at the signal output of the CS circuit at the end of the sampling phase. The sample is held until the resetting phase of the resetting signal begins, and the time interval in between is the holding phase. A sequence of samples are produced when the phases are repeated, and the signal output is the signal output of said CS circuit. The control signal generator 4 has a clock input, which is the clock input of the CS circuit, a sampling signal output connected to the control input of the switch 2 and a resetting signal output connected to the control input of the integrator 3 as mentioned above.--

C5

Pages 7-8, line 25, please replace the paragraph beginning at line 25 with the following:

--The integrator 3 comprises a capacitor 3-1, a resetting switch 3-2 and an optional resistor 3-3 in this embodiment. The integrator 3 can, however, have a different configuration in other embodiments. An analog signal is applied to the input of the sampling switch 2. As described, the charge sampling process involves three successive phases: resetting, sampling (t_1 to t_2) and holding. The time from t_1 to t_2 is defined as the sampling window. FIG. 1B shows its working waveforms. During the resetting phase, only the resetting switch 3-2 is turned on and the capacitor 3-1 is reset. During the sampling phase, only the sampling switch 2 is turned on, and the signal current is integrated onto the capacitor 3-1. The time constant is large enough to be able to obtain a linear charging when the signal comes from a voltage source (the usual case). If the on-resistance of the switch 2 is too small, the optional resistor 3-3 can be added. During the holding phase, both switches are in off-state, and the output voltage of the integrator 3 is held for further use. A pair of interconnected CS circuits, forming a differential CS circuit, provide differential outputs to cancel common mode effects, using a differential input signal and sharing the control signal generator 4. The CS circuits or circuit pairs are used in parallel to increase the sampling rate and to make the time interval between two sampling points possibly less than the sampling window, by time-interleaving both sampling and resetting signals. The signal current can be represented as $I(t) = \Sigma I_i \sin(\omega_i t + \phi_i)$, i=1, 2, ..., m. The total integrated charge is $Q=\Sigma Q_i$ where $Q_i = (I_i/\omega_i)(\cos(\omega_i t_1+\phi_i) - \cos(\omega_i t_2 + \phi_i))$. If t_s is the center time of the sampling window, and $2\Delta t= (t_2-t_1)$ is the window width, $Q_1 = (2\sin(\omega_1\Delta t/\omega_i) I_i \sin(\omega_i t_s + \phi_i) = 2\Delta t (\sin(\omega_i\Delta t)/(\omega_i\Delta t)) I_i \sin(\omega_i t_s + \phi_i)$.--

Pages 11-12, line 16, please replace the paragraph beginning at line 16 as follows:

--A filter function of the BPCS circuits is illustrated in FIG 5. From top-down, the frequency increases from DC to 3f, $_c$ where f_c is the clock frequency. Note that during the negative clock phase the same signal is connected oppositely, which is

reflected in the diagram by changing the signal sign. The normalized amplitudes of resulting charges, i.e. the sums of the areas, integrated in n clock cycles are listed in FIG 5 respectively. It is obvious that for input signals with frequencies much higher or lower than f_c, the charges cancel each other almost completely, resulting in nearly zero output. For input signals with certain frequencies like $f_c/4$, $f_c/2$, $2f_c$, ..., the charges are completely cancelled no matter what their phases are. For input signals with frequencies near f_c, the charges are only partly cancelled. When $f_{in} = f_c$, the charges are fully added to each other if it is in-phase with f_c while fully cancelled when it is in $\pi/2$ phase with f_c (not shown in FIG. 5). There is a bandwidth in which the signal charges can be effectively integrated. Outside the bandwidth, the signal charges are either completely or substantially cancelled. This is obviously a filter function. It means that the noise with frequencies outside the bandwidth will be cancelled as well.--

Pages 12-13, please replace the paragraph beginning at line 27 with the following:

--In FIG 7A and FIG 7B, the ideal frequency responses of a constant-weighting BPCS circuit with n=50 and n=500 are shown respectively. FIG 7A shows the frequency response with n=50 in the range of $0< f_{in} <2f_c$ and in the fine range of $0.95f_c<f_{in}<1.05f_c$. FIG 7B shows the frequency response with n=500 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.995f_c<f_{in}<1.005f_c$. It can be seen that $\Delta f_{3dB}=0.018f_c$ with n=50 and $\Delta f_{3dB}=0.0018f_c$ with n=500, i.e. the bandwidth is inversely proportional to n. The amplitudes of far-end frequency components are reduced with the increase of n, but the maximum adjacent peaks in both cases remain almost unchanged; around -13 dB.--

Page 13, please replace the paragraph beginning at line 4, with the following:

--An ideal frequency responses of a linear-weighting BPCS circuit with n=50 and n=500 are shown in FIG 8A and FIG 8D, respectively. Linear-weighting means that during the sampling phase the weight of the current is first linearly increased and then linearly decreased, symmetric to the center of the sampling window. FIG

SA shows the frequency response with n=50 in the range of $0<f_{in},<2f_c$ and in the fine range of $0.9f_c<f_{in}<1.1f_c$. FIG 8B shows the frequency response with n=500 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.99f_c<f_{in}<1.01f_c$. It can be seen that $\Delta f_{3dB} = 0.025f_c$ with n=50 and $\Delta f_{3dB}=0.0025f_c$ with n=500, slightly increasing compared to the constant-weighting cases. The amplitudes of far-end frequency components are rapidly reduced with the increase of n. The maximum adjacent peaks are reduced to -26 dB and -27 dB respectively, compared to those of the constant-weighting cases.--

Page 14, line 3, please replace the paragraph beginning at line 3 with the following:

--An implementation 14 of the core of the differential BPCS circuit 8, using n-MOS transistors, is shown in FIG 10. The clocked switches are n-MOS transistors 15A, 15B, 15C and 15D. The W&S elements are n-MOS transistors 16A and 16B. The resetting switches are n-MOS transistors 18A and 18B. The capacitors are on-chip MOS capacitors 17A and 17B. The clocks are in sinuous waves but quasi-square waves can also be used. The implementation 14 works in all CMOS processes. Parameters of a 0.8μm CMOS process, however, is used in the HSPICE® simulations. The following three implementations are based on the implementation 14 with particular component values and W&S signal parameters.--

Page 14, line 15, please replace the paragraph beginning at line 15 with the following:

--An implementation 19 with n=10 in constant-weighting at f_c=1000 MHZ is shown in FIG 11A. The clocked switches are n-MOS transistors 20A, 20B, 20C and 20D. The W&S elements are n-MOS transistors 21A and 21B. The resetting switches are n-MOS transistors 23A and 23B. They all have the minimum size, 2 μm/0.8 μm (width/length). The capacitors are MOS capacitors 22A and 22B, both 40 pF. The width of the constant-weighting W&S signal is 10 ns, corresponding to n=10. The maximum differential output sample voltage is around 100 mV. FIG 11B shows both the theoretical frequency response in solid line and the HSPICE®

simulated frequency response in dots for f_{in}=900-1100 MHZ. The simulated frequency response is closely in accordance with the theoretical frequency response. In both cases, the maximum adjacent peaks are -13 dB and Δf_{3dB}=18 MHZ.--

Pages 14-15, line 30, please replace the paragraph beginning at line 30 with the following:

--In FIG 12A, an implementation 24 with n=59 in linear-weighting at f_c=1000 MHZ is shown. The clocked switches are n-MOS transistors 25A, 25B, 25C and 25D, all having an increased size of 10 μm/0.8 μm. This makes the signal currents dominated by the W&S elements not the switches. The W&S elements are n-MOS transistors 21A and 21B, 2 μm/0.8 μm. The resetting switches are n-MOS transistors 23A and 23B, 2 μm/0.8 μm. The capacitors are MOS capacitors 22A and 22B, both 40 pF. The width of the linear-weighting W&S signal is 59 ns, corresponding to n=59. The maximum differential output sample voltage is around 100 mV. FIG 12B shows the theoretical frequency response in solid line and the HSPICE® simulated frequency response in dots for f_{in}=900-1100 MHZ. The simulated frequency response is basically in accordance with the theoretical frequency response. Both have Δf_{3dB} = 2 MHZ. For the implementation 24, however, the maximum adjacent peak is -30 dB, lower than that of the theoretical response. This is because the conductance of n-MOS transistors 21A or 21B does not vary linearly with the linear W&S signal. The actual weighting function is somewhere between linear and Gauss.--

Page 15, line 17, please replace the paragraph beginning at line 17, with the following:

--An implementation 26 with n=599 in linear weighting at f_c=1000 MHZ is shown in FIG 13A. The clocked switches are n-MOS transistors 25A, 25B, 25C and 25D, 10 μm/0.8 μm. The W&S elements are n-MOS transistors 27A and 27B, 2 μm/16 μm. Note that the lengths of 27A and 27B are increased to 16 μm to limit the